Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **VCC**
2. **G=N.A**
3. **A**
4. **H=N.B**
5. **B**
6. **I=N.C**
7. **C**
8. **VSS**
9. **D**
10. **J=N.D**
11. **E**
12. **K=N.E**
13. **F**
14. **L=N.F**

**.060”**

**2 1 14**

**13**

**12**

**11**

**3**

**4**

**5**

**6**

**7 8 9 10**

**4**

**0**

**4**

**9**

**MASK**

**REF**

**.055”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: VCC or Float**

**Mask Ref: 4049**

**APPROVED BY: DK DIE SIZE .055” X .060” DATE: 9/24/18**

**MFG: SPRAGUE/SOLID STATE THICKNESS .020” P/N: CD4049UB**

**DG 10.1.2**

#### Rev B, 7/1